Design Tools for Reconfigurable Hardware in Orbit (RHinO)

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Earth Science Technology Conference

June 23rd, 2004

ESTO

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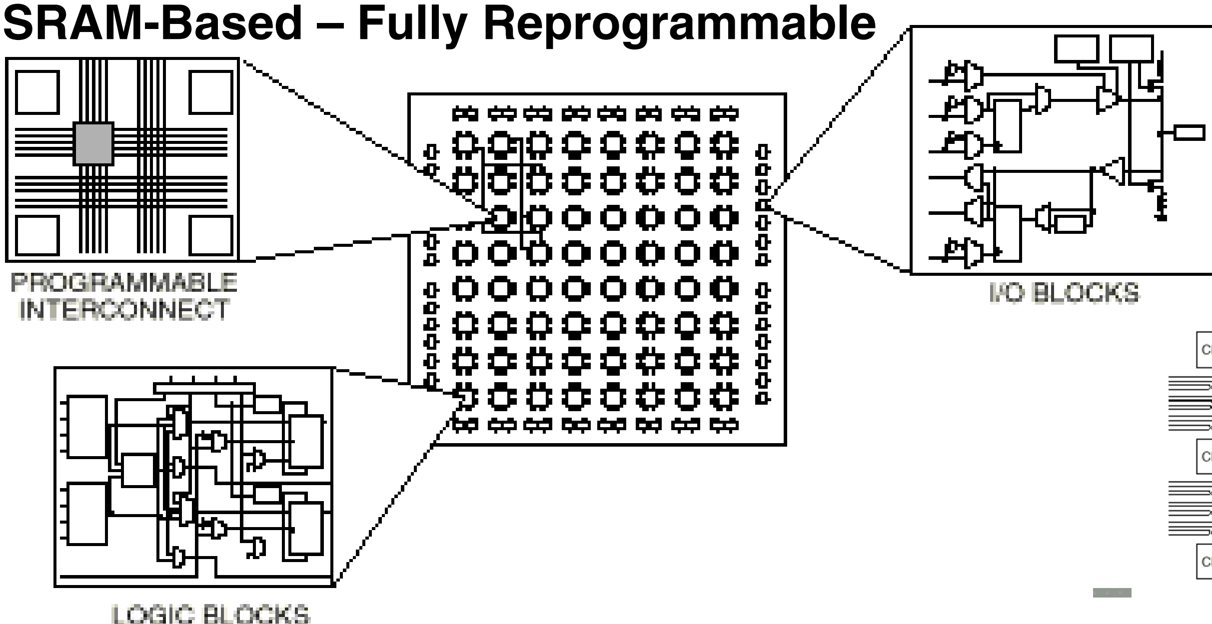
What is an FPGA?

- **Mesh of programmable logic blocks with a programmable interconnect.**
- **Define a “Hardware” circuit using “Software” techniques = Firmware**
- **Two Variants**
  - **Anti-Fuse – One-time Programmable**
  - **SRAM-Based – Fully Reprogrammable**



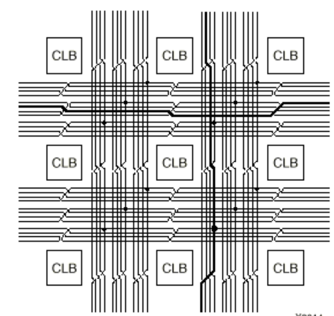
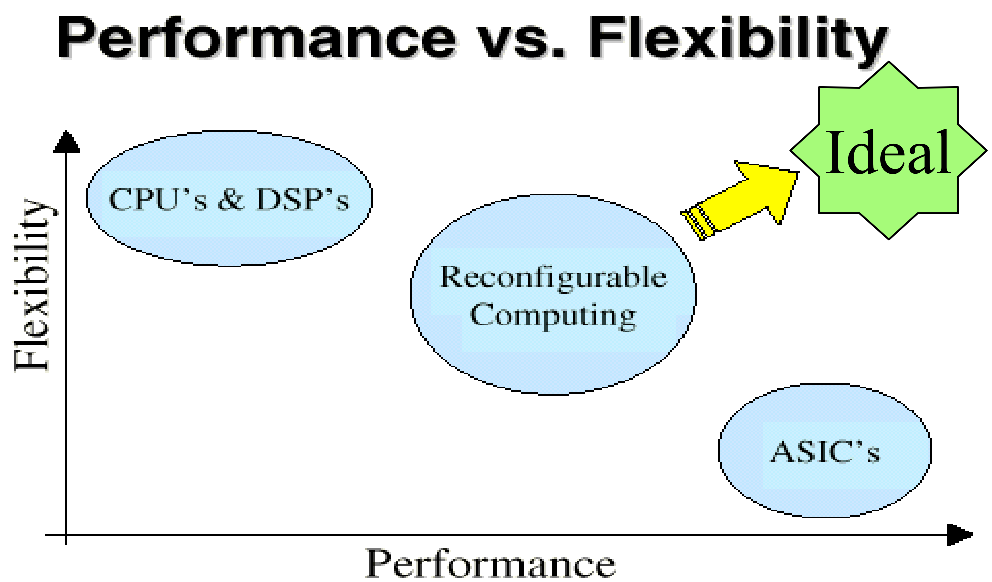


Figure 30: Quad Lines (XC4000X only)

FPGA Niche



"The performance of ASIC's with the flexibility of programmable processors."

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Vs. ASICs:

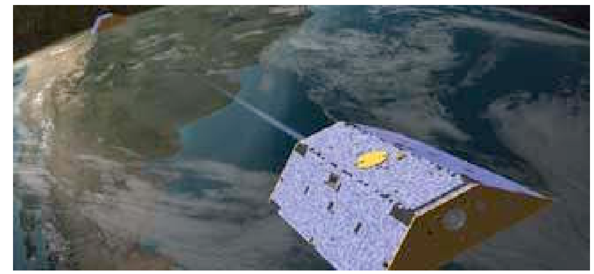
- ☹ ***0.1X power / performance, but…***
- ☺ ***Cheap***
- ☺ ***Rapid design***
- ☺ ***Reprogrammable – "REWIRING IN ORBIT"***
- ➔ ***Lower cost***
- ➔ ***Faster deployment***

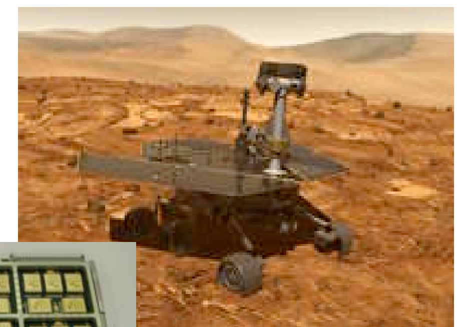
Vs. General-Purpose Processors (GPPs):

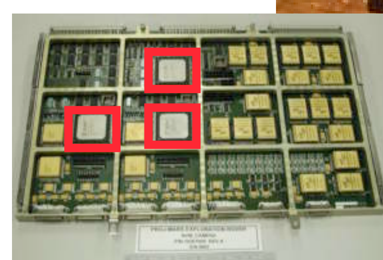
- ☹ ***More expensive***
- ☹ ***Harder to program, but…***
- ☺ ***10-100x power / performance***

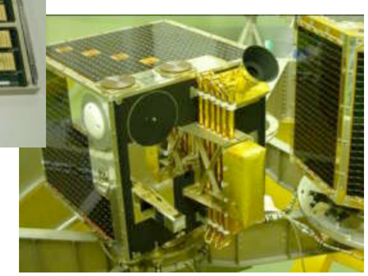
SRAM-Based FPGAs in Space

- **Advantages**
  - 10-100x Processing Performance over Anti-fuse FPGAs
  - Reprogrammable
    - Resource Multiplexing
      - Multi-mission, multi-sensor
    - Mission Obsolescence
      - Update Algorithms
    - Design Flaws
      - Correct in Orbit
- **Gaining Popularity in Space Systems**
  - MARS 2003 Lander (JPL); XQR4062XL
  - MARS 2003 Rover (JPL); XQVR1000
  - GRACE (GSFC); XQR4036XL
  - FedSat (Univ. of Australia); XQR4036XL
  - Optus (Raytheon); XQVR300

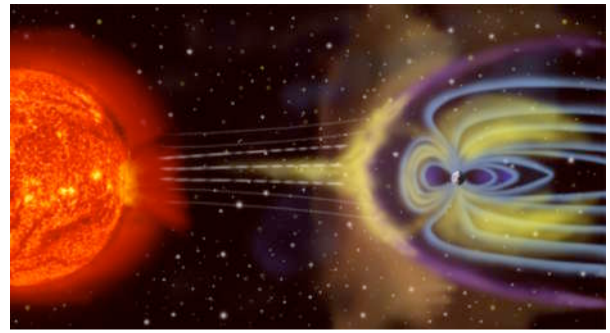








Disadvantages of SRAM-Based FPGAs in Space



- **Radiation Effects**
  - Total Ionizing Dose (TID)
  - Single Event Latchup (SEL)
  - Single Event Upset (SEU)
  - Single Event Functional Interrupt (SEFI)
- **Power**
  - Antifuse is more power savvy
    - Static ~ 20%
    - Dynamic ~50%
  - Greater Horsepower = Greater Power Consumed
- **Currently Addressing Requires**
  - Multiple Ad-hoc tools
  - Expensive Design Techniques (TMR)
  - Elite FPGA Design Team
  - Radiation Hardened Silicon
  - Exhaustive Testing

Can we reduce cost, risk, and design time?

Reconfigurable Hardware IN Orbit (RHINO)

Matthew French, Brian Schott - ISI

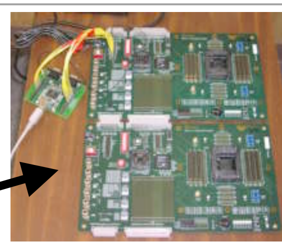
Description and Objectives

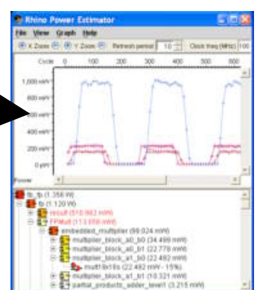
- Facilitate and Automate Designing an SRAM-based FPGA Circuit for the Space Environment
- Create a CAD tool Environment for **Xilinx Virtex-II** SRAM-based FPGAs capable of
  - **Mitigating Transient Effects**
  - **Minimizing Power Utilization**
  - **Evolving around Hard Faults**
- Provide an Extensible Infrastructure for Future Tests, Techniques, and Architectures

Domain Compilers / Power Aware, SEU Cores	Evolvable Hardware		Design Entry
Power & SEU Optimizations			CAD Tools
JHDL CAD Environment			
SEU Analysis	Power Analysis		Analysis, Modeling, & Verification
Space Emulator	Proton Testbed	Power Testbed	

Accomplishments

- Robust EDIF Import Tool
- Half-Latch Removal Tool
- SEU Emulator
- Dynamic Power Visualization
- Detailed Power Analysis Capabilities
- Virtex-II Pre-routed Power Model





Phase	FY03	FY04	FY05
Space Effects and Power Analysis Tools			
Space Effects and Power Optimization Tools			
Radiation Testing and Validation			

- **Image Convolution Benchmark**

$TRL_{in}=3$ ⇒ $TRL_{current}=4$

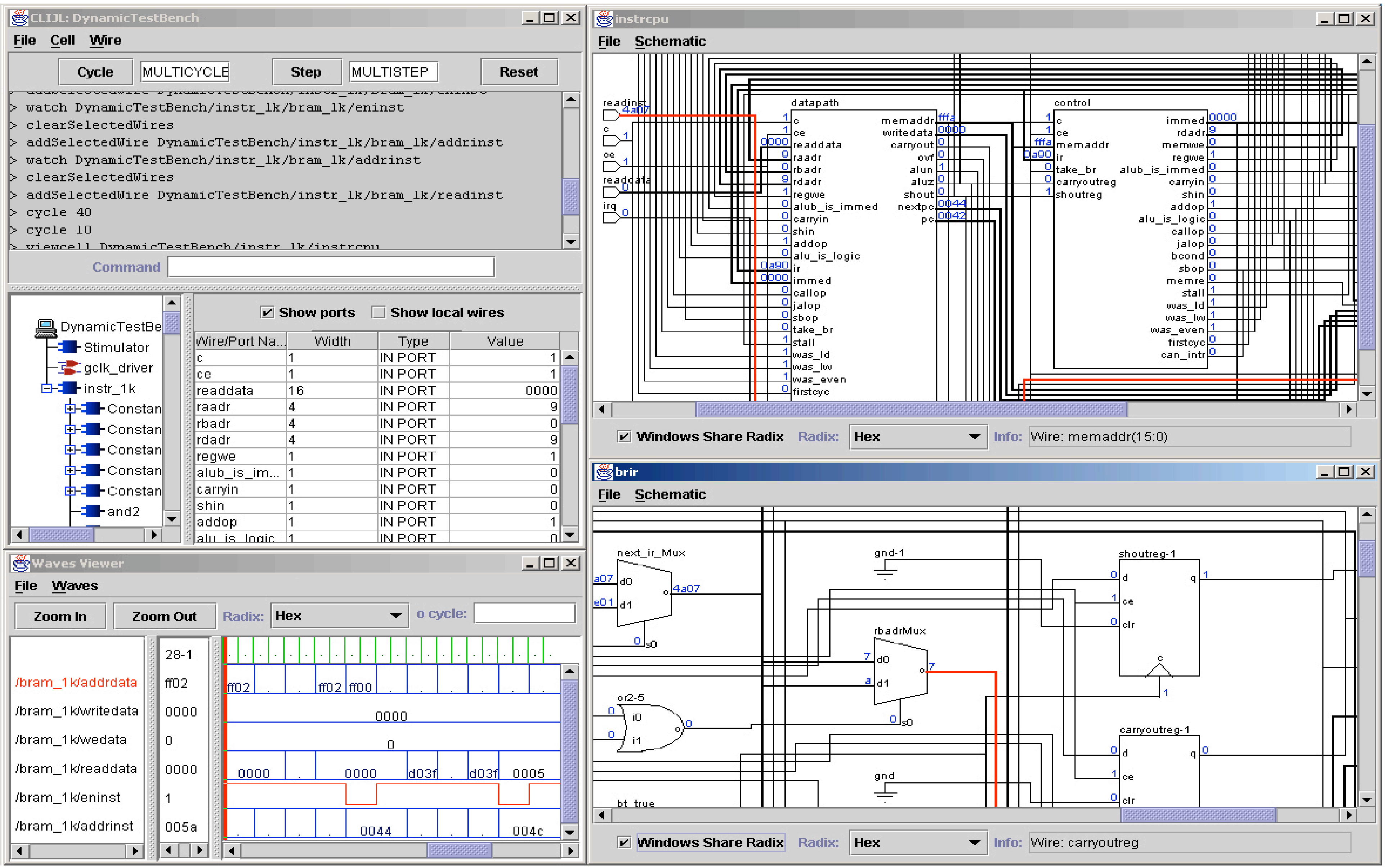
Outline

- JHDL Infrastructure
- Radiation Effects Mitigation
  - Transients
  - Evolvable “Self-Repair” Algorithms
- Power Visualization and Analysis
- Sumary

JHDL Overview

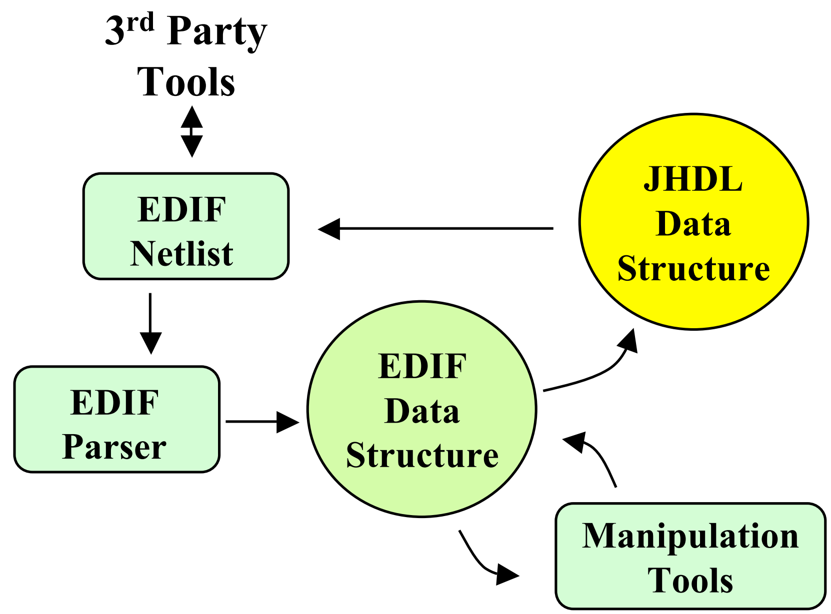
- **Java-based structural design tool for FPGAs**
  - Circuits described by creating Java Classes
    - Instance circuit objects (primitives and modules)
    - Interconnect defined with Wire class objects
  - Design libraries provided for several FPGA families
  - Object Oriented Environment Allows High-level Manipulation of Low-level Circuits
- **JHDL Design Aides**
  - Logic simulator & waveform viewer
  - Circuit schematic & hierarchy browser
  - Module Generators
- **Publicly Available: http://www.jhdl.org**
- **Open Source**
- **Circuit Designer does not need to know Java!**
  - EDIF Import / Export

JHDL Unified Environment



New EDIF Parser

- Supports multiple EDIF files
  - Searches for appropriate EDIF files
  - EDIF *merge* functionality
  - Support for a variety of EDIF styles
- Much more efficient parser
  - Single pass parser
  - Efficient data structure
- JHDL generation
  - Virtex2 libraries and memory initialization
  - Support for "black boxes"
  - No JHDL wrapper required
- EDIF tools distributed via web
  - http://splish.ee.byu.edu/reliability/edif/
  - Several demonstrations are available
    - Visualizing EDIF within JHDL
    - Merging multiple EDIF files

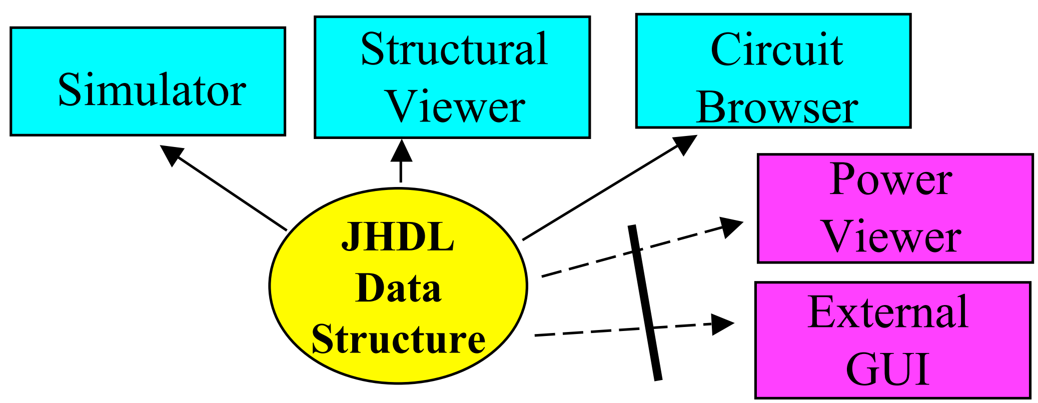


EDIF Tools Verified

- ✓Synplicity 5.x – 7.x
- ✓Synplicity Pro 5.x – 7.x
- ✓Xilinx Coregen 5.x-6.x
- ✓Xilinx System Generator 5.x – 6.x
- ✓Xilinx Chipscope (ILA) 5.x-6.x

JHDL GUI Enhancements

- Support dynamic insertion of 3rd party tools
  - Circuit APIs in place
  - Graphical User Interfaces (GUI) limited
- Current GUI event model limits ability to add interactive tools
  - Hard-coded event interaction model
  - Inability to externally set color of wires/cells etc
- Event Model Restructured
  - Tool Interoperability
  - Cross-probing Enabled
- Key: 3rd Party tools now supported
  - Power Tools Utilizing



Radiation Effects Mitigation

RHinO Fault-Handling Techniques for SRAM-based FPGAs

Radiation-Induced Failure

Characteristics

Duration: Transient | Permanent

Cause: SEU | SEFI | SEL | TID

Approach:

Configuration Scrubbing
Complete TMR

Selective TMR
Half-Latch Removal
Persistence

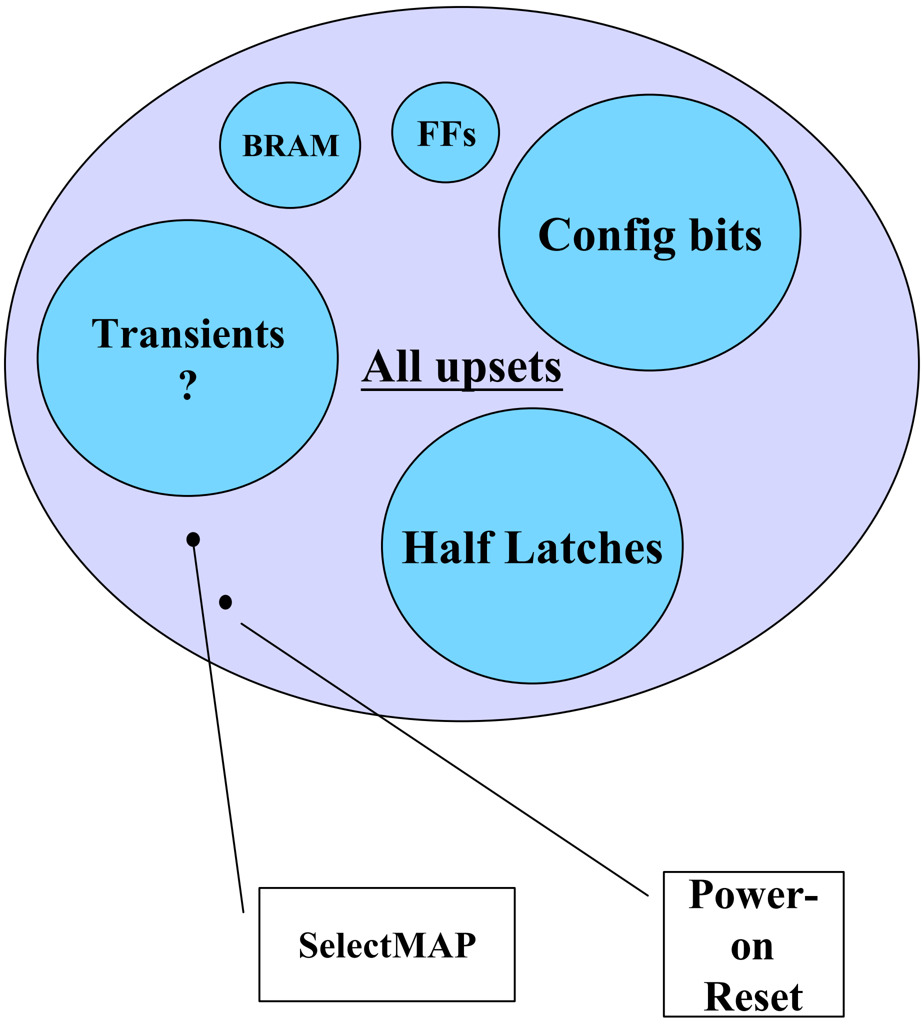
Radiation Hardening

Evolutionary

RHinO Focus

- **Allow Designer to Fit Fault-Handling Level to Need**
- **SEU Emulator**
  - **Increase Effectiveness of Laboratory Level Testing (TRL 4)**
  - **Reduce Time / Cost of Radiation Testing**
- **Evolutionary Techniques**
  - **Add Secondary Insurance to Radiation Hardening**
  - **Potential to move to COTs**
- **Active participant in the Xilinx Radiation Testing Consortium (XRTC)**

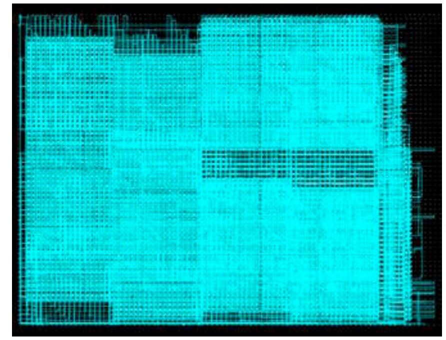
Categories of SEU Sensitive Resources



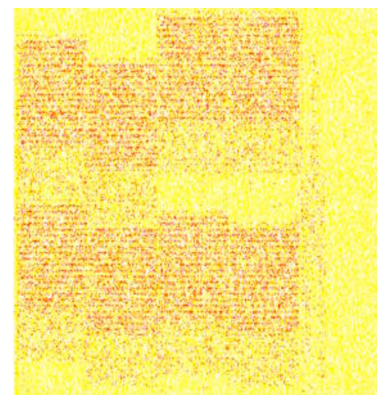
Resource (2V1000)	Sensitive Xsection (cm^2/device)	Relative Feature Size
Configuration bitstream	1.65E-1	76.893%
Block SelectRAM	3.69E-02	17.137%
Flip-flops	1.28E-02	5.965%
Power-on Reset SEFI	6.00E-06	0.003%
SelectMAP SEFI	5.00E-06	0.002%
Half-latches	?	?
Transients	?	?

SEU Characterization/Analysis: SEU Emulation

- **SEU Emulation for Virtex-II**
  - Virtex-II configuration and readback understood as well as Virtex-II bitstream architecture
  - Hardware system
    - COTS FPGA boards (Xilinx AFX)
    - COTS USB interface with custom interface to AFX boards
    - Designs and firmware available to community
  - Software
    - Portable across FPGA architectures, board architectures
    - Allows test designer to specify the type of test to perform
    - Does not expect a "one-size-fits-all" solution to SEU emulation
    - Can be used for SEU emulation or extended to radiation experiments (expanded API)
  - Completion: end of June 2004 (in conjunction with radiation test)

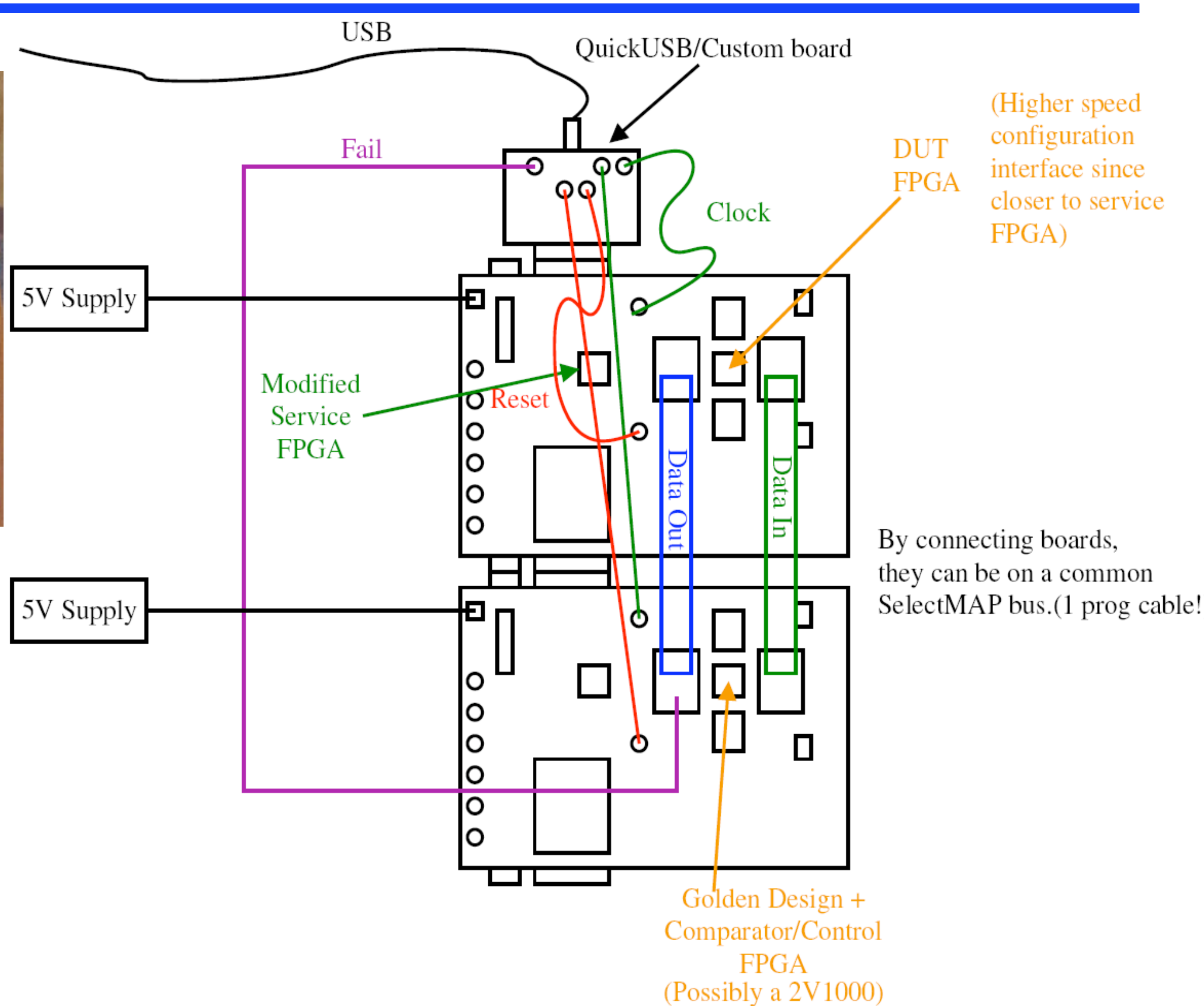


Original Circuit



"Sensitive Bit" Map

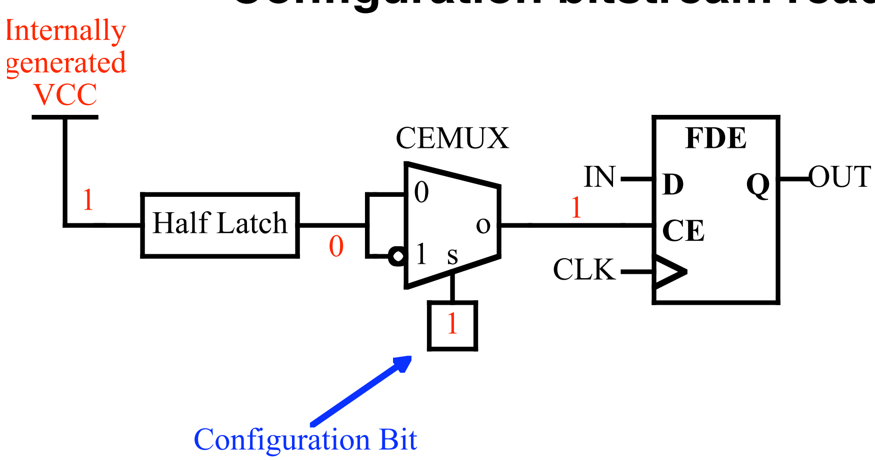
SEU Emulation Hardware (Part II)



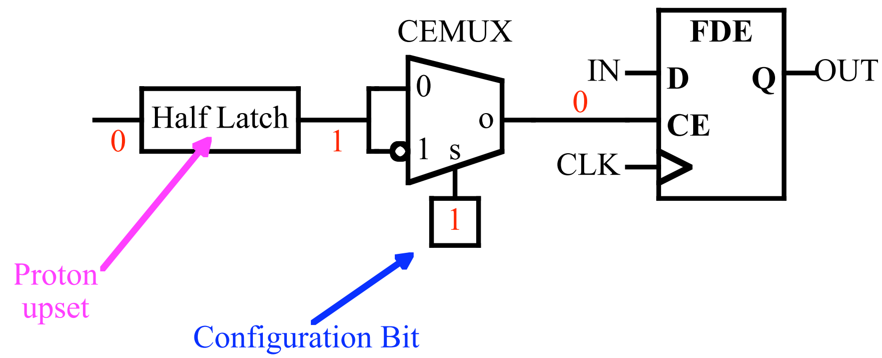
Will also be used for radiation test—dynamic radiation testing very similar to SEU emulation requirements.

Half-Latch SEU

- **Half-latches are low cost resources providing logic “1” or “0” constants in Xilinx FPGA designs.**
- **The half-latch circuit can experience SEUs and will remain upset until full reconfiguration**
- **Partial configuration and bitstream SEU mitigation methods do not help fix.**
- **Configuration bitstream readback will not detect.**



Half-latch initialization with full device configuration (during start-up sequence)



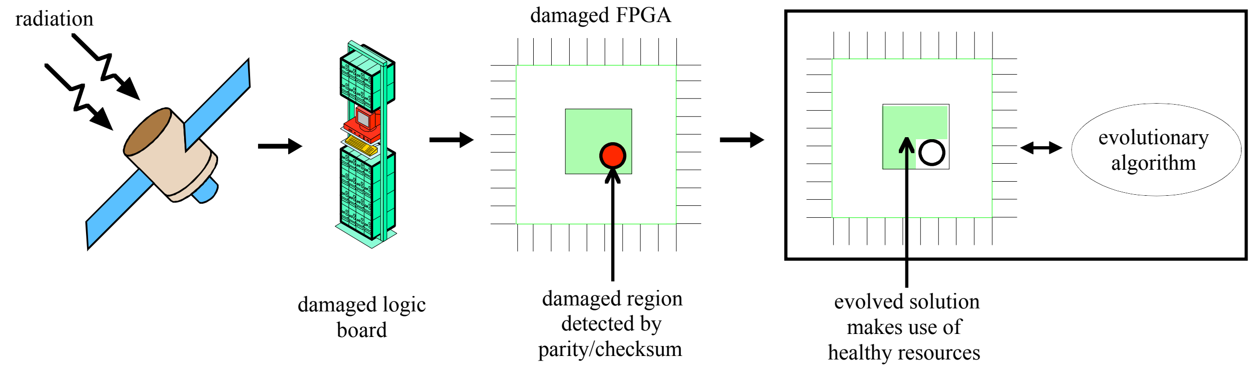
If the half-latch is upset, the flip-flop stops working since the clock enable is not asserted.

RadDRC II

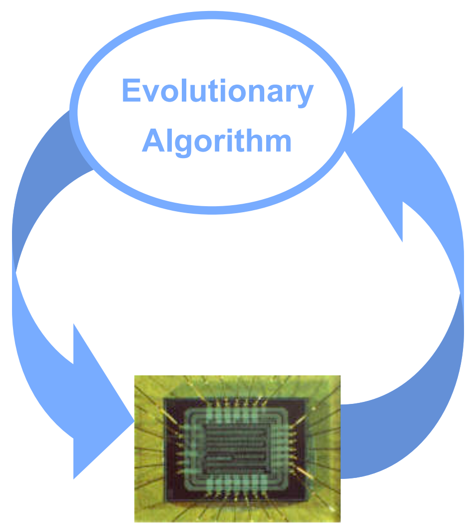
- **Radiation Design Rule Checker for Virtex-II (RadDRC-II)**
  - Implements half-latch SEU analysis and mitigation for Virtex-II designs
- **Has been tested in hardware for correct design operation (USC/ISI Virtex-II Osiris board)**
- **Testing at the proton accelerator June 29-30**
  - Verify Xilinx information about half-latches
  - Compare unmitigated to mitigated designs to better understand the default settings for unused inputs.
- **Impact: Xilinx has added additional half-latch mitigation capabilities to their TMR tool**
- **Licensing**
  - Available now for licensing through the LANL Technology Transfer Office (Government Use and Non-commercial)
  - Working to make the software available open source to ease the licensing process

Fault Recovery

Dynamic Evolution for Fault Tolerance



- **<u>Description</u>:**
  - **Fault tolerance / self-repair in extreme environments**
    - **High temperature**
    - **High radiation**
- **<u>Output</u>: adaptive algorithms for autonomous self-repair of re-programmable logic chips**
- **<u>Target Customer</u>: Aerospace Technology, Space Science, Earth Science Enterprises**
- **<u>Impact</u>: increased safety, autonomy**

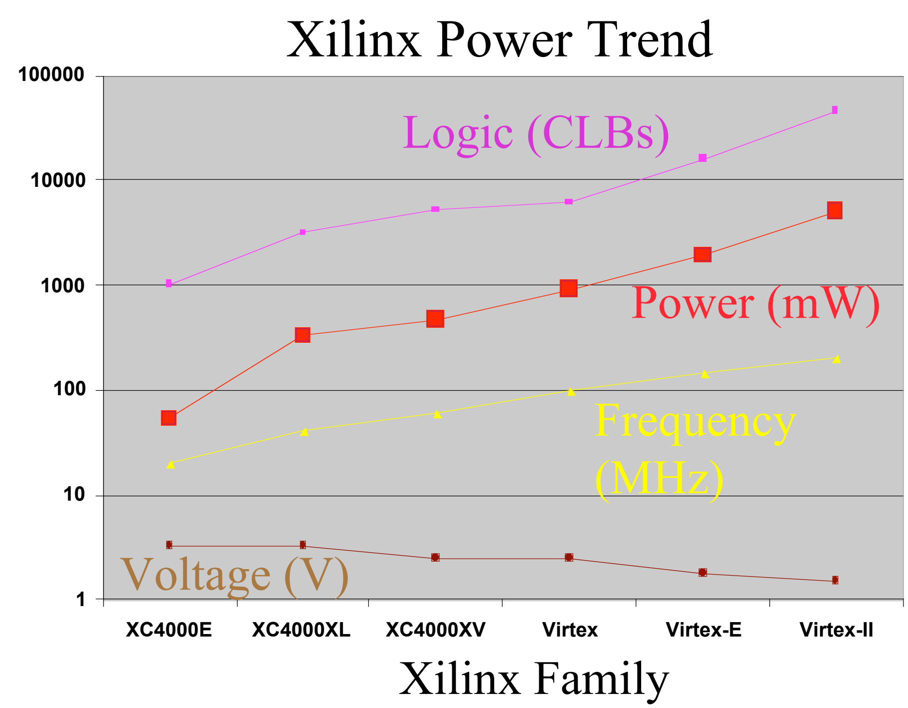


chip reprogrammed by algorithm

Power

RHinO Power Tools

- **Power consumption has become a primary design constraint for some systems, but this is not reflected in modern FPGA tools.**
- **Push power analysis, visualization, and optimization to front of the tools chain:**
  - ***Analyze* power consumption at logic simulation with two levels of accuracy**
    - **Pre-place-and-route, using heuristic estimates based on fanout**
    - **Back-annotated with precise post-place-and-route RC data**
  - ***Visualize* by providing intuitive views to help the designer rapidly find and correct inefficient circuits, operating modes, data patterns, etc.**
  - ***Optimize* systems by automatically identifying problem paths and suggesting improvements**



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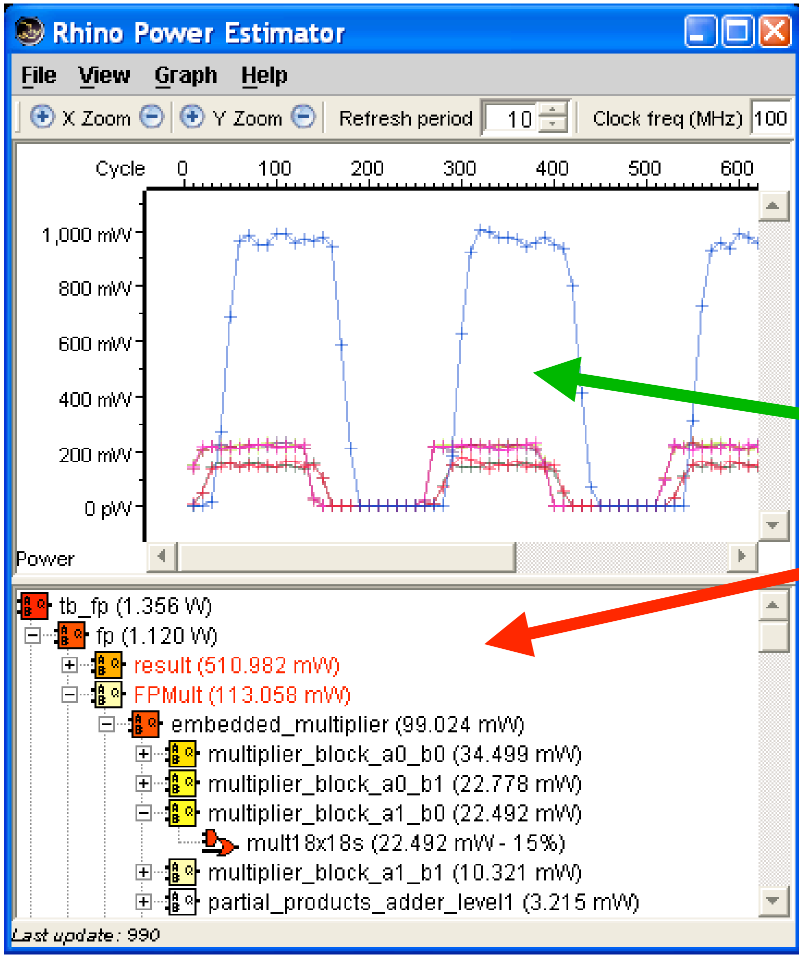
Power Visualization Tool



- **Analysis and visualization tool complete**
- **Power estimation based on one of three Power Models**
  - **Generic Toggle Model**
  - **Virtex II Power Model**
  - **Actual Routed Circuit**
- **Two views:**
  - **Instantaneous vs. cumulative power consumption over time**
  - **Sorted tree view of “worst offenders”**
- **Integrated “cross-probing” with existing JHDL tools**
  - **Unified Environment**
  - **Allows Experimentation**
  - **Smart Re-use of CPU Memory**
- **Help rapidly identify inefficient circuits and operating modes**
- **Per-cell / per-bit granularity**

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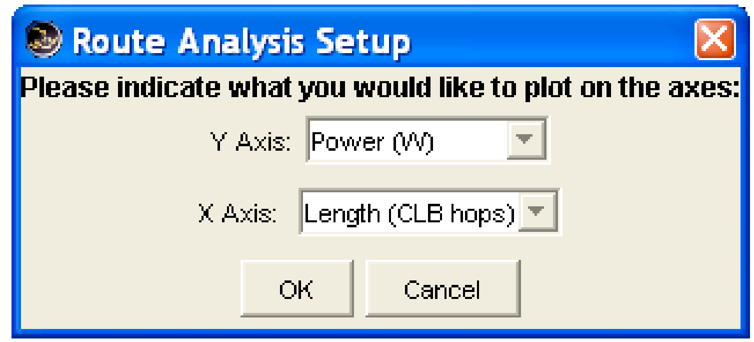
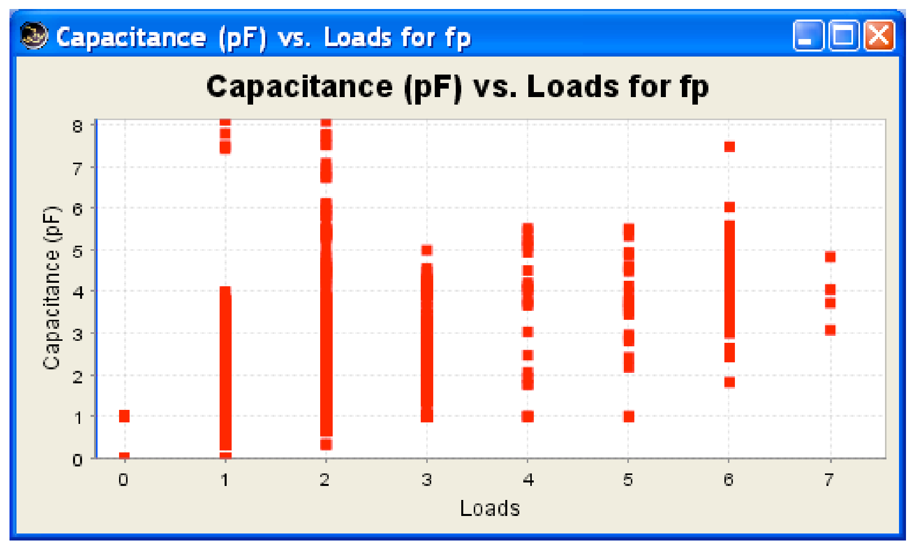
Power Analysis Plot Tool

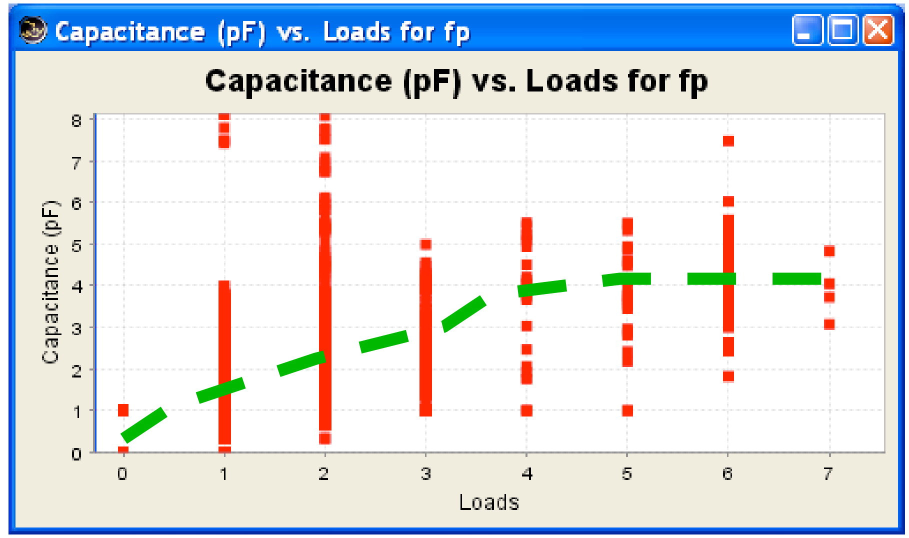
- **Interoperability with Xilinx Tool Flow**
  - **Forward annotation: import JHDL toggle statistics into Xilinx XPower for precise estimation**
  - **Back annotation: import post-layout reports into JHDL for highly accurate estimation as design iterates; analyze routing results for power optimality**
- **Capability to View Route Intrinsics**
  - **Power or Capacitance vs**
  - **Lengths, PIPs, or Loads**
- **Two Critical Uses**
  - **Pre Place and Route Power Models**
  - **Routed Circuit Quality Analysis**

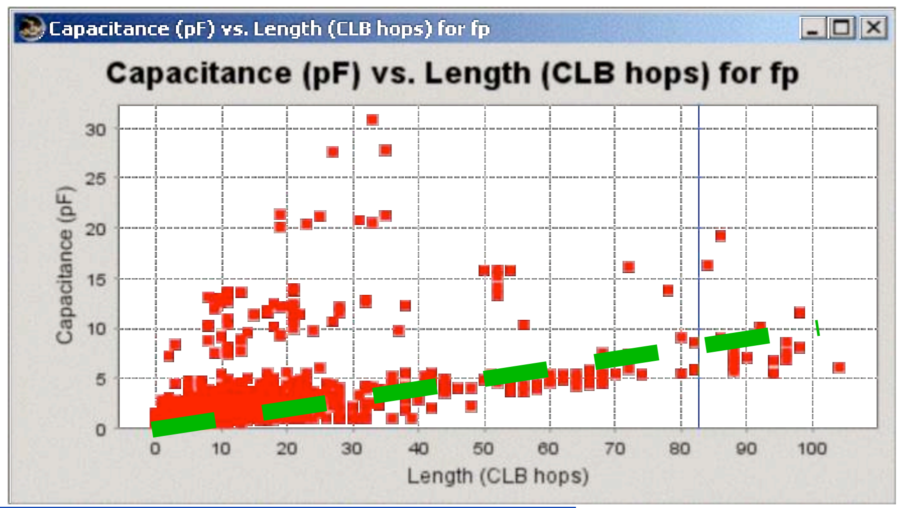




Virtex-II Power Model

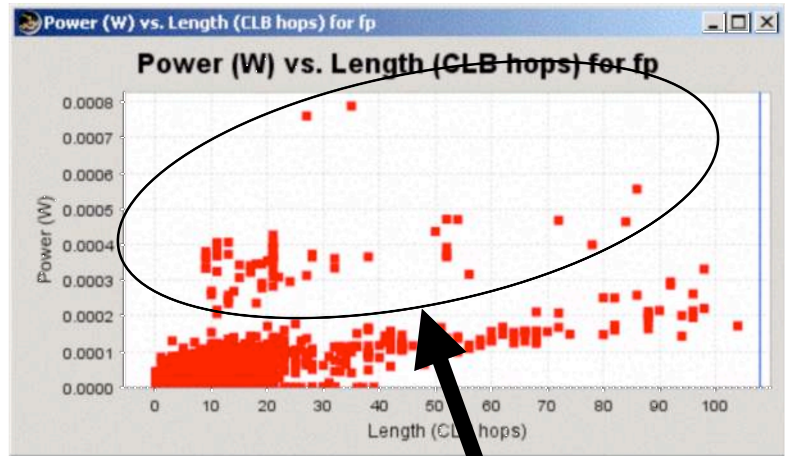
- **How to Estimate Un-Routed Design?**
  - Many signals optimized / combined in Xilinx tool flow
  - What route length / load to use?
- **Back-annotation data used to create detailed Virtex-II power models**
  - Component capacitance
  - Route capacitance estimates based on
    - Fanout
    - Statistical Models
    - Others?
- **Combined with toggle statistics from simulation, provides accurate pre-layout power estimation**



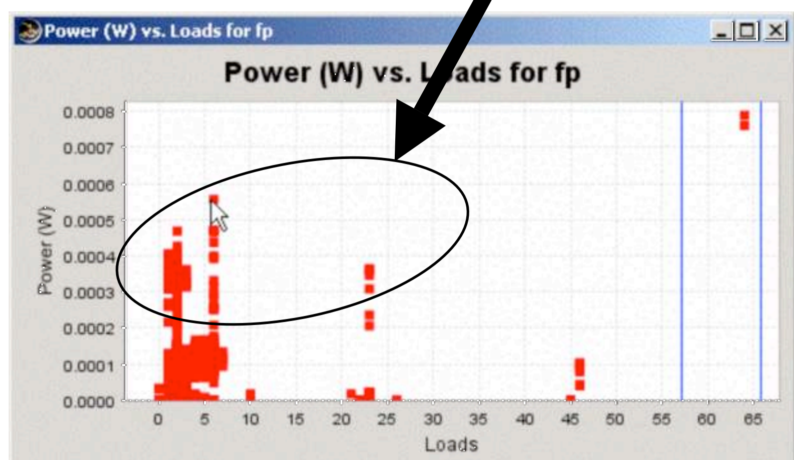


Quality of Routing Analysis

- **Use Power Analysis Tool to Judge Routing Quality**
  - Xilinx Routing algorithm based on timing
  - Now have information on Load, Route as well
  - Identify Outliers
  - Information Available to do Power Weighted Placement and Routing
    - Use Placement Macros in JHDL



Optimization Candidates



Summary

- Significant Progress to Date
  - Automating Radiation Testing
  - Increased Power Visualization
- Future Direction
  - Verifying Tools
    - SEU Emulator
    - Radiation Testing
  - Optimization
    - Radiation - Targeted TMR
    - Power – Intelligent Component Placement
- Tools Available for Distribution
  - EDIF Import Tool
    - http://splish.ee.byu.edu/reliability/edif
    - Open Source
  - Power Tools
    - http://rhino.east.isi.edu (Launching soon!)
    - Open Source
  - RadDRC-II Tool, SEU Emulator
    - Contact LANL
    - Licensing in Progress
  - Unified Distribution Planned